PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-166220
(43)Date of publication of application : 16.06.2000

(51)Int.Cl. H02M 3/07
G02F 1/133
G09G 3/20
G09G 3/36

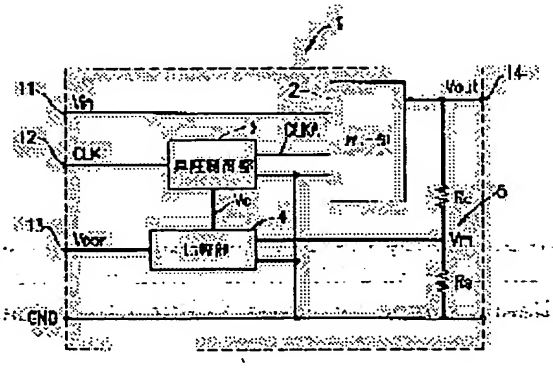
(21)Application number : 11-254972
(22)Date of filing : 08.09.1999

(71)Applicant : SHARP CORP
(72)Inventor : KAJIMOTO KOICHI

(30)Priority
Priority number : 10268743 Priority date : 22.09.1998 Priority country : JP

(54) POWER UNIT, AND DISPLAY AND ELECTRONIC APPARATUS USING THE UNIT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a charge pump system of power circuit which can raise the voltage conversion efficiency and reduce the power consumption and in which the user can set the output voltage optionally.
SOLUTION: A power circuit 1 has a booster 2 which receives the input of input voltage Vin and also receives the input of a clock signal CLKA for boosting and boosts the input voltage Vin to specified output voltage Vout, a voltage dividing circuit 5 which divides the output voltage Vout of this booster 2 by resistors, a comparator 4 which compares the divided voltage Vm generated by this voltage diving circuit 5 with the control voltage Vcon and outputs the result as an output signal Vc, and a boasting controller 3 which receives the input of the output signal Vc and a clock signal VLK1 for operation from the comparator 4 and supplies the clock signal CLKA for boosting to the booster 2.



LEGAL STATUS

[Date of request for examination] 25.01.2002
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number] 3487581
[Date of registration] 31.10.2003

[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

CLAIMS

[Claim(s)]

[Claim 1] The power circuit equipped with the comparator which compares the control voltage which the clock signal for input voltage and pressure ups from a power source is inputted, and is inputted from the pressure-up section which carries out the pressure up of this input voltage to predetermined output voltage, and the output voltage and the outside of this pressure-up section, and carries out the signal output of the result, and the pressure-up control section which the output signal and the clock signal for actuation from this comparator are inputted, and supplies the clock signal for pressure ups to this pressure-up section.

[Claim 2] The power circuit according to claim 1 considered as the configuration which compares with said control voltage the division electrical potential difference which was equipped with the electrical-potential-difference dividing network which carries out resistance division of the output voltage of said pressure-up section, and was generated by this electrical-potential-difference dividing network by said comparator.

[Claim 3] The power circuit according to claim 1 or 2 which will suspend that said pressure-up control section supplies the clock signal for pressure ups to said pressure-up section if it starts that said pressure-up control section will supply the clock signal for pressure ups to said pressure-up section if the result of "Vcon>Vm" is obtained as a comparison result of said comparator and the result of "Vcon<Vm" is obtained as a comparison result of said comparator.

[Claim 4] The power circuit according to claim 1 or 2 which will suspend that said pressure-up control section supplies the clock signal for pressure ups to said pressure-up section if it starts that said pressure-up control section will supply the clock signal for pressure ups to said pressure-up section if the result of "Vcon<Vm" is obtained as a comparison result of said comparator and the result of "Vcon>Vm" is obtained as a comparison result of said comparator.

[Claim 5] The display using the power circuit of one publication among claims 1-4.

[Claim 6] claims 1-4 using the clock signal which carried out dividing of the shift clock signal of the scan line of a line

sequential drive, or it as said clock signal for actuation, and was created ·· the display using the power circuit of one publication.

[Claim 7] Electronic equipment using the power circuit of one publication among claims 1-4.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the display and electronic equipment which used it for the power circuit of the charge pump method which makes it possible to set output voltage as arbitration, and the list while aiming at improvement in electrical potential difference conversion efficiency, and reduction of power consumption.

[0002]

[Description of the Prior Art] In recent years, many liquid crystal displays are used for the display device for a display of OA equipment, such as a word processor and a personal computer, and the AV equipment treating an image, and the list as a display device for information displays of a Personal Digital Assistant. As compared with other display devices, it is because it has the description of a low power for a liquid crystal display by the thin light weight.

[0003] The display device carried in the electronic equipment which supplies power by cells, such as a Personal Digital Assistant and a cellular phone, especially is asked for the further low-power-ization. By these electronic equipment, most power consumption at the time of the standby condition that CPU stops and only the information display is performed depends it on a display device. That is, the time of electronic equipment will be determined by this.

[0004] Many of these electronic equipment makes the cell the power source of supply, and the about [+3V] electrical potential difference is given as a power source for display devices. Here, since an about [+20V] electrical potential difference is needed for driving a liquid crystal display when a liquid crystal display is taken for an example, it is necessary to carry out the pressure up of the electrical potential difference to +20V from +3V in the internal electrical power source circuit of a liquid crystal display. The booster circuit using the transformer as this power circuit and the charge pump type booster circuit using a capacitor are used from the former.

[0005] However, when calling at the booster circuit using a transformer, only about 60% of conversion efficiency was acquired at the maximum, but since especially the liquid crystal display for

Personal Digital Assistants etc. would be used in the low place of the conversion efficiency in a low current load, it had the problem that applicability was restricted.

[0006] For this reason, the booster circuit of the good charge pump method of electrical-potential-difference conversion efficiency attracts attention in the condition with little load current recently. For example, the power circuit of the liquid crystal display which adopted the charge pump method as WO 96/No. 21880 official report is indicated (conventional example 1).

[0007] Generally, in the booster circuit of a charge pump method, in order for the method which accumulates the charge which charged the capacitor to perform a pressure up, output voltage is fixed to the integral multiple of input voltage. For this reason, in order to adjust the display contrast of a liquid crystal display, for example, when making adjustable the electrical potential difference after a pressure up, the method of adjusting an electrical potential difference by variable resistance using a regulator etc. is taken.

[0008] Here, the conventional power circuit which adopted the charge pump method is concretely explained using drawing 8 .

[0009] In this power circuit 81, as shown in drawing 8 , while the clock signal CLK8 for pressure ups is inputted from the clock signal input terminal 85 for pressure ups, input voltage Vin is inputted from the external power terminal 84, and the pressure-up section 82 of a charge pump method outputs the pressure-up electrical potential difference Vsh. While the pressure-up electrical potential difference Vsh from this pressure-up section 82 is inputted, control voltage Vcon is inputted from the terminal 86 for control voltage, and the output voltage Vout of the request whose pressure the armature-voltage control section 83 lowered is outputted.

[0010] In more detail, it can consider as the circuitry shown in drawing 9 R> 9, and the armature-voltage control section 83 is outputting the division electrical potential difference Va obtained by carrying out resistance division of between the terminal 86 for control voltage into which control voltage Vcon is inputted, and the terminals 88 for pressure-up electrical potential differences into which the pressure-up electrical potential difference Vsh from the pressure-up section 82 is inputted by resistance R91 and R92 as output voltage Vout using the voltage follower by the operational amplifier OP (conventional example 2).

[0011]

[Problem(s) to be Solved by the Invention] However, when based on the approach of the conventional example 2 mentioned above, in order to once lower the pressure of and use the potential which carried out the pressure up in the

booster circuit of a charge pump method, a pressure up will be carried out more than a required electrical potential difference, and loss of power will arise. When specifically based on the circuitry shown in drawing 9 , the self-power consumption (Vshxiop) of an operational amplifier will arise from the terminal 88 for pressure-up electrical potential differences too many as loss of a power circuit further with the power {(Vsh-Vcon) xish} by ish which flows toward the terminal 86 for control voltage, and the power {(Vsh-Vout) xiout} for lowering the pressure of Vsh to output voltage Vout.

[0012] Generally, although components, such as a field-effect transistor, are used for switching of a capacitor in the booster circuit of a charge pump method, many of power losses are produced according to the penetration current at the time of switching of this field-effect transistor.

[0013] Moreover, even when using the booster circuit of a charge pump method as a power source, and the load becomes max, it must be considered that descent of output voltage is settled in tolerance. There is a method of enlarging capacity of the capacitor to be used as an approach in this case, or enlarging the frequency of the switching clock signal for pressure ups.

[0014] However, when depending the capacity of a capacitor on the approach of enlarging, it is difficult for reservation of an element-placement field to be difficult and to attain large capacity-ization of a capacitor in the Personal Digital Assistant asked for low-power-izing and a miniaturization.

[0015] Moreover, in depending the frequency of the switching clock signal for pressure ups on the approach of enlarging, the loss at the time of switching becomes large, and electrical-potential-difference conversion efficiency falls. Furthermore, since pressure-up actuation of a charge pump is performed similarly not only at the time of heavy loading but the time of a light load which is close to no-load, there is a problem of also producing the fixed power loss by pressure-up actuation.

[0016] This invention aims at offering the display and electronic equipment which used it for the power circuit of the charge pump method which can set output voltage as arbitration, and the list while it can solve the technical problem of such a conventional technique and can aim at improvement in electrical-potential-difference conversion efficiency, and reduction of power consumption.

[0017]

[Means for Solving the Problem] The pressure-up section to which the clock signal for input voltage and pressure ups from a power source is inputted, and the power circuit of this invention carries out the pressure up of this input voltage to

predetermined output voltage, The comparator which compares the control voltage inputted from the output voltage and the outside of this pressure-up section, and carries out the signal output of the result, The output signal and the clock signal for actuation from this comparator are inputted, it has the pressure-up control section which supplies the clock signal for pressure ups to this pressure-up section, and the above-mentioned purpose is attained by that.

[0018] It is good also as a configuration which compares with said control voltage the division electrical potential difference which was equipped with the electrical-potential-difference dividing network which carries out resistance division of the output voltage of said pressure-up section, and was generated by this electrical-potential-difference dividing network by said comparator.

[0019] If it starts that said pressure-up control section will supply the clock signal for pressure ups to said pressure-up section if the result of "Vcon>Vm" is obtained as a comparison result of said comparator and the result of "Vcon<Vm" is obtained as a comparison result of said comparator, you may suspend that said pressure-up control section supplies the clock signal for pressure ups to said pressure-up section.

[0020] If it starts that said pressure-up control section will supply the clock signal for pressure ups to said pressure-up section if the result of "Vcon<Vm" is obtained as a comparison result of said comparator and the result of "Vcon>Vm" is obtained as a comparison result of said comparator, said pressure-up control section may suspend supplying the clock signal for pressure ups to said pressure-up section.

[0021] The display of this invention may use said power circuit.

[0022] Other displays of this invention may use the shift clock signal of the scan line of a line sequential drive, or the clock signal which carried out dividing of it and created it as said clock signal for actuation.

[0023] The electronic equipment of this invention may use a power circuit.

[0024] Below, an operation of this invention is explained.

[0025] According to the above-mentioned configuration, a comparator compares the control voltage inputted from the output voltage and the outside of the pressure-up section, the signal output of that result is carried out, a pressure-up control section operates according to the clock signal for actuation, the clock signal for pressure ups based on the output signal from a comparator is supplied to the pressure-up section, and the pressure-up section carries out the pressure up of the input voltage from a power source to predetermined output

voltage based on this clock signal for pressure ups. For this reason, it becomes possible to set output voltage as arbitration with control voltage, using a charge pump method. Moreover, since a pressure-up control section controls actuation of the pressure-up section and does not perform the pressure up beyond the need based on the output signal from a comparator, it becomes possible to perform optimal pressure-up actuation corresponding to a load characteristic. Therefore, it becomes possible to aim at improvement in the electrical-potential-difference conversion efficiency of the whole power circuit, and reduction of power consumption.

[0026] Moreover, it has the electrical-potential-difference dividing network which carries out resistance division of the output voltage of the pressure-up section, it becomes possible, if the division electrical potential difference generated by this electrical-potential-difference dividing network and control voltage are made the configuration compared by the comparator to control actuation of the pressure-up section by low control voltage, and it becomes possible to aim at reduction of much more power consumption in a power circuit.

[0027] Moreover, by using the above-mentioned power circuit for a display and electronic equipment, it becomes possible to reduce the power consumption of a display and electronic equipment, and it becomes possible to develop a battery life and to lengthen usable time amount.

[0028] In addition, if it is made the configuration using the shift clock signal of the scan line of a line sequential drive, or the clock signal which carried out dividing of it and created it as the above-mentioned clock signal for actuation, it is not necessary to newly prepare a clock signal generating circuit, and it will become possible to reduce the part power consumption.

[0029]

[Embodiment of the Invention] Below, the gestalt of operation of this invention is concretely explained based on a drawing.

[0030] (Operation gestalt 1) As the power circuit 1 by this invention is for driving a liquid crystal display and is shown in drawing 1 The pressure-up section 2 which clock signal CLKA for pressure ups is inputted while input voltage Vin is inputted from the external power input terminal 11, and carries out the pressure up of the input voltage Vin to the predetermined output voltage Vout, The electrical-potential-difference dividing network 5 which carries out resistance division of the output voltage Vout of this pressure-up section 2, The division electrical potential difference Vm and the control voltage Vcon from the control volt input terminal 13 which were generated by this electrical-potential-difference

dividing network 5 are compared. It has the comparator 4 which outputs that result as an output signal Vc, and the pressure-up control section 3 which the output signal Vc and the clock signal CLK1 for actuation from this comparator 4 are inputted, and supplies clock signal CLKA for pressure ups to the pressure-up section 2.

[0031] Here, before giving explanation about the detail of the above-mentioned power circuit 1, the pressure-up approach by the booster circuit of a charge pump method is first explained using drawing 2 and drawing 3 .

[0032] Drawing 2 (a) simplifies and shows the switch section 20 used for a booster circuit, with a clock signal CLK2, it is changing a switch 21 to H side edge child or L side edge child, and the potential VH of the high-tension side or the potential VL of the low-tension side produces it in input/output terminal VI/O. The switch section 20 can be made into the circuitry shown in drawing 2 (b), and, as for diode, and R1 and R2, for C1 and C2, more specifically, resistance, and Q1 and Q2 are [a coupling capacitor, and D1 and D2] field-effect transistors. When the signal inputted into CLK2 terminal is set to "High", a field-effect transistor Q1 turns on this switch section 20, and the potential VH of the high-tension side produces it in input/output terminal VI/O. At this time, a field-effect transistor Q2 is OFF. On the other hand, when the signal inputted into CLK2 terminal is set to "Low", a field-effect transistor Q2 turns on, and the potential VL of the low-tension side arises in input/output terminal VI/O. At this time, a field-effect transistor Q1 is OFF.

[0033] While the configuration of the booster circuit 30 which used this switch section 20 is shown and input voltage Vin is inputted from the volt input terminal 31, drawing 3 The high-tension-side switch section 34 and the low-tension side switch section 35 which the clock signal CLK3 for pressure ups is inputted from the clock signal input terminal 32 for pressure ups, and perform switching operation, It has the premature start capacitor 36 for pressure ups and the capacitor 37 for an output which are changed by the switching operation of those switch sections 34 and 35. Using these capacitors 36 and 37, the pressure up of the input voltage Vin is carried out, and the predetermined output voltage Vout is outputted to an output terminal 33.

[0034] If input voltage Vin is inputted into the volt input terminal 31 and CLK3 signal of "Low" is first inputted into the clock signal input terminal 32 for pressure ups in more detail, the high-tension-side switch section 34 and the low-tension side switch section 35 will be connected to the terminal by the side of L by switching operation. Therefore, input voltage Vin is impressed to the

premature start capacitor 36 for pressure ups, and a charge is stored. Next, if CLK3 signal of "High" is inputted into the clock signal input terminal 32 for pressure ups, the high-tension-side switch section 34 and the low-tension side switch section 35 will be connected to the terminal by the side of H by switching operation. At this time, the premature start capacitor 36 for pressure ups and the capacitor 37 for an output are connected electrically, and the charge charged in previous actuation by the premature start capacitor 36 for pressure ups is sent to the capacitor 37 for an output. When pressure-up actuation is performed and pressure-up actuation is repeated with the proper clock signal CLK3 for pressure ups by repeating this actuation, in an output terminal 33, input voltage twice the electrical potential difference of Vin arises as output voltage Vout.

[0035] Next, the concrete configuration of the power circuit 1 of this invention shown in drawing 1 is explained in detail using drawing 4 - drawing 6 .

[0036] The pressure-up section 2 of a charge pump method enables it to perform a 8 times as many pressure up as this at the maximum to input voltage Vin combining the three same booster circuits 41, 42, and 43 as the booster circuit 30 of drawing 3 mentioned above, as shown in drawing 4 . Generally this is because about +20V is needed to input voltage Vin being about +3V as driver voltage of the liquid crystal display used for a Personal Digital Assistant in a Personal Digital Assistant. The pressure-up control section 3 consists of the AND gates 61, as shown in drawing 6 , and the comparator 4 consists of comparators 51, as shown in drawing 5 . The resistance Rc and Rs shown in drawing 1 is division resistance for creating the reference voltage for a liquid crystal drive using the output voltage from the pressure-up section 2, and set the resistance ratio to Rc:Rs=15:1 here.

[0037] First, actuation of the pressure-up section 2 is explained. It is the same as that of the booster circuit 30 of drawing 3 mentioned above as pressure-up actuation, and as shown in drawing 4 , while input voltage Vin is supplied from the volt input terminal 44, clock signal CLKA for pressure ups is inputted into the 1st step booster circuit 41 from the clock signal input terminal 45 for pressure ups, and, specifically, a charge is transmitted to it from the premature start capacitor CF 1 for pressure ups to the capacitor CC 1 for an output by the switching operation of high-tension-side switch section S1H and low-tension side switch section S1L. Here, when pressure-up actuation is repeated by proper clock signal CLKA for pressure ups, the electrical potential difference VA of 2xVin arises at the A point shown in drawing 4 .

[0038] Next, clock signal CLKA for

pressure ups is inputted into the 2nd step booster circuit 42 from the clock signal input terminal 45 for pressure ups, and a charge is transmitted to it from the premature start capacitor CF 2 for pressure ups to the capacitor CC 2 for an output by the electrical potential difference produced at the A point by the switching operation of high-tension-side switch section S2H and low-tension side switch section S2L being changed suitably. Here, when pressure-up actuation is repeated by proper clock signal CLKA for pressure ups, the electrical potential difference VB of 4xVin arises at the B point shown in drawing 4 .

[0039] Next, clock signal CLKA for pressure ups is inputted into the 3rd step booster circuit 43 from the clock signal input terminal 45 for pressure ups, and a charge is transmitted to it from the premature start capacitor CF 3 for pressure ups to the capacitor CC 3 for an output by the electrical potential difference produced at the B point by the switching operation of high-tension-side switch section S3H and low-tension side switch section S3L being changed suitably. Here, when pressure-up actuation is repeated by proper clock signal CLKA for pressure ups, for the voltage-output terminal 46 shown in drawing 4 , the electrical potential difference of 8xVin arises as output voltage Vout. Thus, the output voltage Vout by which the pressure up of the input voltage Vin was increased 8 times is obtained by the pressure-up section 2 shown in drawing 1 .

[0040] Next, actuation of a comparator 4 is explained. It consists of circuits shown by drawing 5 (a), the division electrical potential difference Vm obtained by carrying out resistance division of the output voltage Vout by which the pressure up was carried out in the pressure-up section 2 by Resistance Rc and Rs, and control voltage Vcon are inputted, and this comparator 4 compares both with a comparator 51, and outputs that result as a signal Vc. As actuation of this comparator 51 is shown in the table of drawing 5 (b), at the time of Vcon>Vm, an output signal Vc serves as "High" and an output signal Vc serves as "Low" at the time of Vcon<Vm. Although the circumference circuit was omitted and shown here, in order to suppress the deflection of an output Vc in fact, as Vw shows, a certain amount of hysteresis is given to the comparator 51 by the circumference circuit at drawing 7 (d).

[0041] Next, actuation of the pressure-up control section 3 is explained. This pressure-up control section 3 consists of the AND gates 61, as shown in drawing 6 , takes AND of the clock signal CLK1 for actuation, and the output signal Vc of a comparator 4, and outputs clock signal CLKA for pressure ups. In addition, although the AND gate was raised as an example here, components, such as

NAND, OR, and NOR, may be used with the polarity of an input signal etc.

[0042] Here, according to actuation of each part mentioned above, actuation of the power circuit 1 whole is explained sequentially from a power up. First, suppose that input voltage Vin (for example, +3V), the clock signal CLK1 (refer to drawing 7 (a)) for actuation, and control voltage Vcon (for example, +1V) were inputted into the power circuit 1 shown in drawing 1 . At this time, since the pressure-up section 2 is not operating, output voltage Vout is 0V. Therefore, the division electrical potential difference Vm is also 0V. Therefore, a comparator 4 performs the electrical-potential-difference comparison of control voltage Vcon and the division electrical potential difference Vm, and since it is Vcon>Vm, it outputs the "High" signal as an output signal Vc. The clock signal CLK1 for actuation passes the pressure-up control section 3, and is inputted into the pressure-up section 2 by this. Thereby, the pressure-up section 2 starts pressure-up actuation, and output voltage Vout rises. Therefore, the division electrical potential difference Vm also rises. The division electrical potential difference Vm continues a rise until it exceeds the potential (for example, +1V) of control voltage Vcon. In addition, since the division electrical potential differences Vm are 1/16 of electrical potential differences of output voltage Vout, output voltage Vout continues a rise until it exceeds +16V.

[0043] Next, when it becomes Vcon<Vm, the output signal Vc of a comparator 4 changes to the "Low" signal (refer to drawing 7 (b)). Then, the clock signal CLK1 for actuation is omitted by the pressure-up control section 3, and suspends actuation of the pressure-up section 2. Thereby, the rise of output voltage Vout stops, and it falls until output voltage Vout declines gradually with the discharge property by the capacitor CC 3 and load which are shown in drawing 4 in the last stage of the pressure-up section 2 and, as for output voltage Vout, the division electrical potential difference Vm is less than the value of control voltage Vcon. By repeating these actuation, as shown in drawing 7 (d), the division electrical potential difference Vm operates so that it may be settled between width of face **(1/2) Vw(s) of the value of control voltage Vcon, and a hysteresis. In addition, this electrical potential difference Vw was set up so that a liquid crystal display might not be affected. Moreover, as shown in drawing 7 R> 7 (c), clock signal CLKA for pressure ups has stopped the period shown with Sign S and Sign T, and pressure-up actuation is not performed. Therefore, loss of the power by switching is not generated, either.

[0044] As well as the above when

changing the value of control voltage Vcon, the division electrical potential difference Vm operates so that it may be settled between width-of-face **(1/2) Vw(s) of the value of control voltage Vcon, and a hysteresis. For this reason, the relation of following the (1) type is always realized, and control voltage about 16 times the electrical potential difference of Vcon is outputted to output voltage Vout.

[0045]

Vcon=Vm=(1/16) Vout .... (1)

That is, output voltage Vout of a charge pump circuit can be made adjustable. Moreover, when a load becomes large by the case where the display pattern of liquid crystal changes etc., or also when a load becomes small conversely, the relation of the above-mentioned (1) formula is maintained by the same actuation, and since pressure-up actuation according to the load at that time is performed, loss of power is reduced.

[0046] Moreover, since the self-consumed electric current used the thing of several microA order and used the input voltage Vin of +3V as a power source of a comparator, the power loss in this load circuit of the comparator 51 of a comparator 4 is 1% or less of the whole power consumption.

[0047] (Operation gestalt 2) The booster circuit of each stage was controlled by said operation gestalt 1 to coincidence using the clock CLKA for pressure ups. However, this invention can be carried out also by controlling a part of booster circuit.

[0048] Below, the power circuit 150 in the operation gestalt 2 is explained using drawing 10 .

[0049] Drawing 10 is drawing showing the block of the power circuit 150 in the operation gestalt 2. The power circuit 150 is equipped with the pressure-up section 106, the pressure-up control section 107, and the comparator 108. With the operation gestalt 2, it differs from said operation gestalt 1 that the clock signal CLK1 for actuation is inputted not only into the pressure-up control section 107 but into the pressure-up section 106.

[0050] Drawing 11 is drawing showing the detail of the pressure-up section 106.

[0051] The pressure-up section 106 is equipped with the 1st step booster circuit 111, the 2nd step booster circuit 112, and the 3rd step booster circuit 113.

[0052] In the pressure-up section 2 of said operation gestalt 1, although clock signal CLKA for pressure ups was inputted into all pressure-up stages, in the pressure-up section 106 of the operation gestalt 2, clock signal CLKA for pressure ups is inputted only into the 3rd step booster circuit 113, and the clock signal CLK1 for actuation is inputted into the 1st step booster circuit 111 and the 2nd step booster circuit 112.

[0053] Drawing 12 is drawing showing the clock signal CLK1 for actuation, clock

signal CLKA for pressure ups, etc.

[0054] As shown in drawing 12, the clock signal CLK1 for actuation is a signal not stopping while the power circuit 150 is operating. For this reason, in the circuitry of the operation gestalt 2, the 1st step booster circuit 111 and the 2nd step booster circuit 112 are always operating, the electrical potential difference of 2xVin appears in the point A shown in drawing 11, and 4xVin appears in the point B shown in drawing 11.

[0055] Moreover, the clock CLKA for pressure ups is inputted into the 3rd step booster circuit 113 like the operation gestalt 1, and intermittent pressure-up actuation is performed only in this 3rd step booster circuit.

[0056] Since the pressure-up stage which performs an intermittent control action turns into only the last stage while there is a demerit that the adjustable range of output voltage Vout becomes narrow by the circuit shown in drawing 10 and drawing 11 from "0V-24V" of said operation gestalt 1 to "12V-24V", there is a merit that generating of the ripple voltage accompanying pressure-up actuation is suppressed compared with the case where all pressure-up stages perform an intermittent control action (output voltage is stabilized).

[0057] Moreover, if the driver voltage of a liquid crystal display component is usually more than 12V, since it is good, the above-mentioned demerit will not pose a problem as a matter of fact.

[0058] Although the hysteresis characteristic was given to the comparator 4 with said operation gestalt 1 since the ripple voltage of Vm potential shown in drawing 10 by suppressing generating of the ripple voltage accompanying pressure-up actuation was also stopped, a comparator without the hysteresis characteristic shown in drawing 5 can be used.

[0059] As mentioned above, drawing 12 is drawing showing the wave of the signal of the power circuit 150 of the operation gestalt 2 of operation.

[0060] A different place from said operation gestalt 1 is to perform timing which supplies or stops the clock CLKA for pressure ups in the place which the potential of Vcon and Vm reverses.

[0061] However, since pressure-up actuation is performed for a while also immediately after becoming Vcon<Vm under the effect of the time delay t by the comparator used as a comparator 108, and the switching element of the pressure-up section 106, the potential of Vm rises until the clock CLKA for pressure ups stops, and starts to descend after that.

[0062] Since pressure-up actuation is not performed immediately after becoming Vcon>Vm similarly for the time being, it descends until the clock CLKA for pressure ups is inputted, and changes to the Gokami **.

[0063] These actuation has [gestalt / 1 / said / operation / this example] large generating of the ripple voltage accompanying pressure-up actuation in output voltage. This is for all pressure-up stages to operate to coincidence, or to stop. For this reason, it is desirable to restrict the upper limit and minimum of a ripple voltage by the comparator which gave the hysteresis. However, generating of the ripple voltage by the pressure-up actuation which influences output voltage can be suppressed by carrying out the intermittent control action only of the last pressure-up stage like the configuration of this example, and the output voltage stabilized even if it used what does not have a hysteresis for the configuration of a comparator 108 like drawing 5 is obtained.

[0064] If it sees in the viewpoint of power consumption, since only a step [3rd] pressure-up stage performs an intermittent control action with this operation gestalt to all pressure-up stages performing the intermittent control action and other pressure-up stages are always operating, with said operation gestalt 1, it will be thought from a viewpoint of power consumption that this operation gestalt is disadvantageous. However, even in a step [2nd] pressure-up stage, the electrical potential difference by which the pressure up was carried out is below an electrical potential difference required for a liquid crystal display (liquid crystal is driven), it is that even the step [2nd] pressure-up stage is always operating, and the stop time of the intermittent control action of a step [3rd] pressure-up stage becomes long. For this reason, if it sees in the whole booster circuit, the big difference to power consumption will not be seen by this operation gestalt and the 1st operation gestalt.

[0065] Here, along with the configuration of an accompanying drawing, explanation of operation was given for circuit actuation of Vcon, the potential difference of Vm, and the circumference for convenience. For this reason, pressure-up actuation is started by Vcon<Vm, and when it is Vcon>Vm, pressure-up actuation stops. However, it is satisfactory even if it makes it a reverse configuration depending on the logical organization of a comparator and a pressure-up control section.

[0066]

[Effect of the Invention] According to the power circuit of this invention, as explained above, a comparator compares the control voltage inputted from the output voltage and the outside of the pressure-up section, the signal output of that result is carried out, a pressure-up control section operates according to the clock signal for actuation, the clock signal for pressure ups based on the output signal from a comparator is supplied to the pressure-up section, and the

pressure-up section carries out the pressure up of the input voltage from a power source to predetermined output voltage based on this clock signal for pressure ups. For this reason, output voltage can be set as arbitration with control voltage, using a charge pump method. Moreover, since a pressure-up control section controls actuation of the pressure-up section and does not perform the pressure up beyond the need based on the output signal from a comparator, optimal pressure-up actuation corresponding to a load characteristic can be performed. Therefore, improvement in the electrical-potential-difference conversion efficiency of the whole power circuit and reduction of power consumption can be aimed at.

[0067] Moreover, it has the electrical-potential-difference dividing network which carries out resistance division of the output voltage of the pressure-up section, and if the division electrical potential difference generated by this electrical-potential-difference dividing network and control voltage are made the configuration compared by the comparator, actuation of the pressure-up section can be controlled by low control voltage, and reduction of much more power consumption can be aimed at in a power circuit.

[0068] Moreover, by using the above-mentioned power circuit for a display and electronic equipment, the power consumption of a display and electronic equipment can be reduced, a battery life can be developed, and usable time amount can be lengthened.

[0069] In addition, if it is made the configuration using the shift clock signal of the scan line of a line sequential drive, or the clock signal which carried out dividing of it and created it as the above-mentioned clock signal for actuation, it is not necessary to newly prepare a clock signal generating circuit, and the part power consumption can be reduced.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the configuration of the power circuit of this invention.

[Drawing 2] It is drawing showing the switch section used for the power circuit of this invention, and (a) is schematic drawing and the (b) circuit diagram.

[Drawing 3] It is drawing showing an example of the booster circuit of a charge pump method.

[Drawing 4] It is drawing showing the example of a circuit of the pressure-up section in the power circuit of this invention.

[Drawing 5] It is drawing showing the

comparator in the power circuit of this invention, and is the table where (a) expresses a circuit diagram and (b) expresses operating state.

[Drawing 6] It is drawing showing the example of a circuit of the pressure-up control section in the power circuit of this invention.

[Drawing 7] It is the timing diagram which shows actuation of the power circuit of this invention.

[Drawing 8] It is the block diagram showing the configuration of the conventional power circuit.

[Drawing 9] It is drawing showing the example of a circuit of the armature-voltage control section in the conventional power circuit.

[Drawing 10] It is drawing showing the block of the power circuit 150 in the operation gestalt 2.

[Drawing 11] It is drawing showing the detail of the pressure up section 106.

[Drawing 12] It is drawing showing the wave of the signal of the power circuit 150 of the operation gestalt 2 of operation.

[Description of Notations]

1 Power Circuit

2 Pressure-Up Section

3 Pressure-Up Control Section

4 Comparator

5 Electrical-Potential-Difference Dividing Network

20 Switch Section

30 Booster Circuit

34, S1H, S2H, and S3H High-tension-side switch section

35, S1L, S2L, and S3L Low-tension side switch section

36 CF1, CF2, CF3 Premature start capacitor

37 CC1, CC2, CC3 Capacitor for an output

41 1st Step Booster Circuit

42 2nd Step Booster Circuit

43 3rd Step Booster Circuit

51 Comparator

61 AND-Gate Circuit

Vin Input voltage

Vout Output voltage

Vcon Control voltage

Vm Division electrical potential difference

Vc The output signal of a comparator

CLK1 Clock signal for actuation

CLKA, CLK3 Clock signal for pressure ups

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2000－166220
（P2000－166220A）
(43)公開日　平成12年６月16日(2000.6.16)

(51)Int.Cl.'		識別記号	FI		テーマコード'(参考)
Ｈ０２Ｍ	3/07		Ｈ０２Ｍ	3/07	
Ｇ０２Ｆ	1/133	５２０	Ｇ０２Ｆ	1/133	５２０
Ｇ０９Ｇ	3/20	６１１	Ｇ０９Ｇ	3/20	６１１Ａ
	3/36			3/36	

審査請求　未請求　請求項の数７　ＯＬ　（全９頁）

(21)出願番号　特願平11－254972

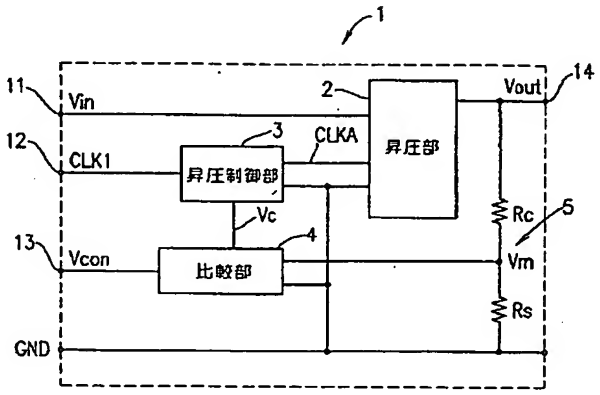
(22)出願日　平成11年９月８日(1999.9.8)

(31)優先権主張番号　特願平10－268743
(32)優先日　平成10年９月22日(1998.9.22)
(33)優先権主張国　日本（ＪＰ）

(71)出願人　000005049
シャープ株式会社
大阪府大阪市阿倍野区長池町22番22号
(72)発明者　梶本　耕市.
大阪府大阪市阿倍野区長池町22番22号　シャープ株式会社内
(74)代理人　100078282
弁理士　山本　秀策

(54)【発明の名称】　電源回路それを用いた表示装置及び電子機器

(57)【要約】
【課題】　電圧変換効率の向上及び消費電力の低減を図ることができると共に、出力電圧を任意に設定することができるチャージポンプ方式の電源回路、並びにそれを用いた表示装置及び電子機器を提供する。
【解決手段】　電源回路１を、入力電圧Ｖｉｎが入力されると共に昇圧用クロック信号ＣＬＫＡが入力され、入力電圧Ｖｉｎを所定の出力電圧Ｖｏｕｔに昇圧する昇圧部２と、この昇圧部２の出力電圧Ｖｏｕｔを抵抗分割する電圧分割回路５と、この電圧分割回路５により生成された分割電圧Ｖｍと制御電圧Ｖｃｏｎとを比較して、その結果を出力信号Ｖｃとして出力する比較部４と、この比較部４からの出力信号Ｖｃ及び動作用クロック信号ＣＬＫ１が入力され、昇圧用クロック信号ＣＬＫＡを昇圧部２に供給する昇圧制御部３とを有する構成とする。



【００２８】加えて、上記動作用クロック信号として、線順次駆動の走査ラインのシフトクロック信号、又はそれを分周して作成したクロック信号を用いる構成にすると、クロック信号発生回路を新たに設ける必要がなく、その分消費電力を低減することが可能となる。

【００２９】

【発明の実施の形態】以下に、本発明の実施の形態を図面に基づいて具体的に説明する。

【００３０】（実施形態１）本発明による電源回路１は、例えば液晶表示装置を駆動するためのものであって、図１に示すように、外部電源入力端子１１から入力電圧Ｖｉｎが入力されると共に昇圧用クロック信号ＣＬＫＡが入力され、入力電圧Ｖｉｎを所定の出力電圧Ｖｏｕｔに昇圧する昇圧部２と、この昇圧部２の出力電圧Ｖｏｕｔを抵抗分割する電圧分割回路５と、この電圧分割回路５により生成された分割電圧Ｖｍと制御電圧入力端子１３からの制御電圧Ｖｃｏｎとを比較して、その結果を出力信号Ｖｃとして出力する比較部４と、この比較部４からの出力信号Ｖｃ及び動作用クロック信号ＣＬＫ１が入力され、昇圧用クロック信号ＣＬＫＡを昇圧部２に供給する昇圧制御部３とを有する。

【００３１】ここで、上記の電源回路１の詳細についての説明をする前に、まずチャージポンプ方式の昇圧回路による昇圧方法を、図２及び図３を用いて説明する。

【００３２】図２（ａ）は、昇圧回路に用いるスイッチ部２０を簡略化して示しており、クロック信号ＣＬＫ２により、スイッチ２１をＨ側端子又はＬ側端子に切り替えることで、高圧側の電位V_H又は低圧側の電位V_Lが入出力端子$V_{I/O}$に生じる。より具体的には、スイッチ部２０は例えば図２（ｂ）に示す回路構成とすることができ、Ｃ１，Ｃ２は結合コンデンサ、Ｄ１，Ｄ２はダイオード、Ｒ１，Ｒ２は抵抗、Ｑ１，Ｑ２は電界効果トランジスタである。このスイッチ部２０は、ＣＬＫ２端子に入力される信号が“Ｈｉｇｈ”になったとき電界効果トランジスタＱ１がＯＮし、高圧側の電位V_Hが入出力端子$V_{I/O}$に生じる。このとき電界効果トランジスタＱ２はＯＦＦである。他方、ＣＬＫ２端子に入力される信号が“Ｌｏｗ”になったとき電界効果トランジスタＱ２がＯＮし、低圧側の電位V_Lが入出力端子$V_{I/O}$に生じる。このとき電界効果トランジスタＱ１はＯＦＦである。

【００３３】図３は、このスイッチ部２０を用いた昇圧回路３０の構成を示しており、電圧入力端子３１から入力電圧Ｖｉｎが入力されると共に、昇圧用クロック信号入力端子３２から昇圧用クロック信号ＣＬＫ３が入力されスイッチング動作を行う高圧側スイッチ部３４及び低圧側スイッチ部３５と、それらのスイッチ部３４、３５のスイッチング動作によって切り替えられる昇圧用フライングコンデンサ３６及び出力用コンデンサ３７とを有し、これらのコンデンサ３６、３７を用いて、入力電圧Ｖｉｎを昇圧し、出力端子３３に所定の出力電圧Ｖｏｕｔを出力する。

【００３４】より詳しくは、まず、電圧入力端子３１に入力電圧Ｖｉｎが入力され、昇圧用クロック信号入力端子３２に“Ｌｏｗ”のＣＬＫ３信号が入力されると、高圧側スイッチ部３４及び低圧側スイッチ部３５はスイッチング動作によりＬ側の端子に接続される。従って、昇圧用フライングコンデンサ３６には入力電圧Ｖｉｎが印加され、電荷が蓄えられる。次に、昇圧用クロック信号入力端子３２に“Ｈｉｇｈ”のＣＬＫ３信号が入力されると、高圧側スイッチ部３４及び低圧側スイッチ部３５はスイッチング動作によりＨ側の端子に接続される。このとき、昇圧用フライングコンデンサ３６と出力用コンデンサ３７は電気的に接続され、先の動作で昇圧用フライングコンデンサ３６に充電された電荷は出力用コンデンサ３７へ送られる。この動作を繰り返すことによって昇圧動作が行われ、適正な昇圧用クロック信号ＣＬＫ３で昇圧動作を繰り返した場合、出力端子３３には出力電圧Ｖｏｕｔとして入力電圧Ｖｉｎの２倍の電圧が生じる。

【００３５】次に、図１に示した本発明の電源回路１の具体的構成を図４～図６を用いて詳しく説明する。

【００３６】チャージポンプ方式の昇圧部２は、図４に示すように、上述した図３の昇圧回路３０と同じ３つの昇圧回路４１、４２、４３を組み合わせて、入力電圧Ｖｉｎに対し最大で８倍の昇圧を行えるようにしている。これは、一般に携帯情報端末では入力電圧Ｖｉｎが＋３Ｖ程度であるのに対し、携帯情報端末に用いられる液晶表示装置の駆動電圧として＋２０Ｖ程度を必要とするためである。昇圧制御部３は、図６に示すようにＡＮＤゲート６１で構成されており、比較部４は、図５に示すようにコンパレータ５１で構成されている。図１に示す抵抗Ｒｃ、Ｒｓは、昇圧部２からの出力電圧を用いて液晶駆動用の基準電圧を作成するための分割抵抗であり、ここではその抵抗比をＲｃ：Ｒｓ＝１５：１とした。

【００３７】まず、昇圧部２の動作を説明する。昇圧動作としては上述した図３の昇圧回路３０と同様であり、具体的には、図４に示すように、第１段昇圧回路４１には、電圧入力端子４４から入力電圧Ｖｉｎが供給されると共に、昇圧用クロック信号入力端子４５から昇圧用クロック信号ＣＬＫＡが入力され、高圧側スイッチ部$S1_H$及び低圧側スイッチ部$S1_L$のスイッチング動作により、昇圧用フライングコンデンサＣＦ１から出力用コンデンサＣＣ１へ電荷が転送される。ここで、適正な昇圧用クロック信号ＣＬＫＡにより昇圧動作を繰り返した場合には、図４に示すＡ点には２×Ｖｉｎの電圧V_Aが生じる。

【００３８】次に、第２段昇圧回路４２には、昇圧用クロック信号入力端子４５から昇圧用クロック信号ＣＬＫＡが入力され、高圧側スイッチ部$S2_H$及び低圧側スイッチ部$S2_L$のスイッチング動作により、Ａ点に生じた

電圧が適宜切り替えられることで、昇圧用フライングコンデンサＣＦ２から出力用コンデンサＣＣ２へ電荷が転送される。ここで、適正な昇圧用クロック信号ＣＬＫＡにより昇圧動作を繰り返した場合には、図４に示すＢ点には４×Ｖｉｎの電圧V_Bが生じる。

【００３９】次に、第３段昇圧回路４３には、昇圧用クロック信号入力端子４５から昇圧用クロック信号ＣＬＫＡが入力され、高圧側スイッチ部$S3_H$及び低圧側スイッチ部$S3_L$のスイッチング動作により、Ｂ点に生じた電圧が適宜切り替えられることで、昇圧用フライングコンデンサＣＦ３から出力用コンデンサＣＣ３へ電荷が転送される。ここで、適正な昇圧用クロック信号ＣＬＫＡにより昇圧動作を繰り返した場合には、図４に示す電圧出力端子４６には出力電圧Ｖｏｕｔとして８×Ｖｉｎの電圧が生じる。このようにして、図１に示す昇圧部２によって、入力電圧Ｖｉｎが８倍に昇圧された出力電圧Ｖｏｕｔが得られる。

【００４０】次に、比較部４の動作を説明する。この比較部４は、例えば図５（ａ）で示す回路で構成されており、昇圧部２で昇圧された出力電圧Ｖｏｕｔを抵抗Ｒｃ、Ｒｓにより抵抗分割して得られる分割電圧Ｖｍと、制御電圧Ｖｃｏｎとが入力され、コンパレータ５１で両者を比較し、その結果を信号Ｖｃとして出力する。このコンパレータ５１の動作は、図５（ｂ）の表に示すように、Ｖｃｏｎ＞Ｖｍのとき出力信号Ｖｃは“Ｈｉｇｈ”となり、Ｖｃｏｎ＜Ｖｍのときは出力信号Ｖｃは“Ｌｏｗ”となる。ここでは周辺回路を省略して示したが、実際には出力Ｖｃの振れを抑えるため、周辺回路により、図７（ｄ）にＶｗで示すように、コンパレータ５１にある程度のヒステリシスを持たせている。

【００４１】次に、昇圧制御部３の動作を説明する。この昇圧制御部３は、例えば図６に示すようにＡＮＤゲート６１で構成されており、動作用クロック信号ＣＬＫ１と比較部４の出力信号ＶｃのＡＮＤをとって昇圧用クロック信号ＣＬＫＡを出力する。尚、ここではＡＮＤゲートを例としてあげたが、入力信号の極性等によっては、ＮＡＮＤ、ＯＲ、ＮＯＲ等の素子を用いてもよい。

【００４２】ここで、上述した各部の動作に従って電源回路１全体の動作を電源投入時から順に説明する。まず、図１に示す電源回路１に、入力電圧Ｖｉｎ（例えば＋３Ｖ）、動作用クロック信号ＣＬＫ１（図７（ａ）参照）、制御電圧Ｖｃｏｎ（例えば＋１Ｖ）が入力されたとする。このとき、昇圧部２は動作していないので出力電圧Ｖｏｕｔは０Ｖである。よって分割電圧Ｖｍも０Ｖである。従って、比較部４は制御電圧Ｖｃｏｎと分割電圧Ｖｍの電圧比較を行い、Ｖｃｏｎ＞Ｖｍであるので出力信号Ｖｃとして“Ｈｉｇｈ”信号を出力する。これによって動作用クロック信号ＣＬＫ１は昇圧制御部３を通過して昇圧部２に入力される。これにより昇圧部２は昇圧動作を開始し、出力電圧Ｖｏｕｔは上昇する。よって分割電圧Ｖｍも上昇する。分割電圧Ｖｍは制御電圧Ｖｃｏｎの電位（例えば＋１Ｖ）を越えるまで上昇を続ける。尚、分割電圧Ｖｍは出力電圧Ｖｏｕｔの１／１６の電圧なので、出力電圧Ｖｏｕｔは＋１６Ｖを越えるまで上昇を続ける。

【００４３】次に、Ｖｃｏｎ＜Ｖｍとなったとき、比較部４の出力信号Ｖｃは“Ｌｏｗ”信号に変わる（図７（ｂ）参照）。すると動作用クロック信号ＣＬＫ１は昇圧制御部３でカットされ昇圧部２の動作は停止する。これにより、出力電圧Ｖｏｕｔの上昇は停止し、昇圧部２の最終段にある図４に示すコンデンサＣＣ３と負荷による放電特性によって出力電圧Ｖｏｕｔは徐々に低下し、出力電圧Ｖｏｕｔは分割電圧Ｖｍが制御電圧Ｖｃｏｎの値を下回るまで低下していく。これらの動作を繰り返すことによって、分割電圧Ｖｍは、図７（ｄ）に示すように、制御電圧Ｖｃｏｎの値とヒステリシスの幅±（１／２）Ｖｗの間に収まるように動作する。尚、この電圧Ｖｗは液晶表示に影響が出ないように設定した。また、図７（ｃ）に示すように、符号Ｓと符号Ｔで示す期間は昇圧用クロック信号ＣＬＫＡが停止しており昇圧動作が行われていない。よって、スイッチングによる電力の損失も発生しない。

【００４４】制御電圧Ｖｃｏｎの値を変化させた場合も、上記と同様にして分割電圧Ｖｍは制御電圧Ｖｃｏｎの値とヒステリシスの幅±（１／２）Ｖｗの間に収まるように動作する。このため、下記（１）式の関係が常に成り立ち、出力電圧Ｖｏｕｔには制御電圧Ｖｃｏｎの約１６倍の電圧が出力される。

【００４５】

$$Vcon = Vm = (1/16)\,Vout \cdots (1)$$

つまり、チャージポンプ回路の出力電圧Ｖｏｕｔを可変とすることができる。また、液晶の表示パターンが変わった場合などで負荷が大きくなった場合や逆に負荷が小さくなった場合にも、同様の動作により上記（１）式の関係が保たれ、そのときの負荷に応じた昇圧動作が行われるため電力の損失は低減される。

【００４６】また、比較部４のコンパレータ５１は、自己消費電流が数μＡオーダーのものを使用し、コンパレータの電源としては例えば＋３Ｖの入力電圧Ｖｉｎを使用したため、この負荷回路における電力損失は全体の消費電力の１％以下である。

【００４７】（実施形態２）前記実施形態１では、昇圧用クロックＣＬＫＡを用いて各段の昇圧回路を同時に制御した。しかしながら、昇圧回路の一部を制御することによっても、本発明を実施することができる。

【００４８】以下に、実施形態２における電源回路１５０を図１０を用いて説明する。

【００４９】図１０は、実施形態２における電源回路１５０のブロックを示す図である。電源回路１５０は、昇圧部１０６と、昇圧制御部１０７と、比較部１０８とを

備えている。実施形態２では、動作用クロック信号ＣＬＫ１が昇圧制御部１０７だけでなく昇圧部１０６にも入力されていることが前記実施形態１と異なる。

【００５０】図１１は、昇圧部１０６の詳細を示す図である。

【００５１】昇圧部１０６は、第１段昇圧回路１１１と、第２段昇圧回路１１２と、第３段昇圧回路１１３とを備えている。

【００５２】前記実施形態１の昇圧部２では、昇圧用クロック信号ＣＬＫＡが全ての昇圧段に入力されていたが、実施形態２の昇圧部１０６では、昇圧用クロック信号ＣＬＫＡが第３段昇圧回路１１３のみに入力されており、第１段昇圧回路１１１と第２段昇圧回路１１２には動作用クロック信号ＣＬＫ１が入力されている。

【００５３】図１２は、動作用クロック信号ＣＬＫ１及び昇圧用クロック信号ＣＬＫＡなどを示す図である。

【００５４】図１２に示すように、動作用クロック信号ＣＬＫ１は、電源回路１５０が動作している間、停止しない信号である。このため、実施形態２の回路構成では、第１段昇圧回路１１１と第２段昇圧回路１１２は常に動作しており、図１１に示す点Ａには２×Ｖｉｎの電圧が現われ、図１１に示す点Ｂには４×Ｖｉｎが現われる。

【００５５】また、第３段昇圧回路１１３には、実施形態１と同様に昇圧用クロックＣＬＫＡが入力されており、間欠昇圧動作はこの第３段昇圧回路でのみで行われる。

【００５６】図１０及び図１１に示す回路によって、出力電圧Ｖｏｕｔの可変範囲は、前記実施形態１の「０Ｖ～２４Ｖ」から「１２Ｖ～２４Ｖ」へと狭くなるというデメリットがある反面、間欠動作を行う昇圧段が最終段だけになるので、全ての昇圧段が間欠動作を行う場合に比べて昇圧動作に伴うリップル電圧の発生が抑えられる（出力電圧が安定する）というメリットがある。

【００５７】また、液晶表示素子の駆動電圧は通常１２Ｖ以上であればよいため、前述のデメリットは事実上問題とはならない。

【００５８】昇圧動作に伴うリップル電圧の発生を抑えることにより、図１０に示すＶｍ電位のリップル電圧も抑えられるため、前記実施形態１では比較部４にヒステリシス特性を持たせていたが、図５に示すヒステリシス特性を持たない比較部を用いることができる。

【００５９】上述したように、図１２は、実施形態２の電源回路１５０の信号の動作波形を示す図である。

【００６０】前記実施形態１と異なるところは、昇圧用クロックＣＬＫＡを供給或いは停止させるタイミングをＶｃｏｎとＶｍの電位が反転するところで行っていることにある。

【００６１】ただし、比較部１０８として使用されるコンパレータと、昇圧部１０６のスイッチング素子による遅延時間ｔの影響でＶｃｏｎ＜Ｖｍになった直後もしばらく昇圧動作が行われるため、Ｖｍの電位は昇圧用クロックＣＬＫＡが停止するまで上昇し、その後下降に転じる。

【００６２】同様にＶｃｏｎ＞Ｖｍとなった直後もしばらくは昇圧動作が行われないため、昇圧用クロックＣＬＫＡが入力されるまで下降し、その後上昇に転じる。

【００６３】これらの動作は前記実施形態１では、出力電圧が本実施例に比べ昇圧動作に伴うリップル電圧の発生が大きい。これは、全ての昇圧段が同時に動作したり停止したりするためである。このため、ヒステリシスを持たせた比較部によってリップル電圧の上限と下限を制限することが望ましい。しかし本実施例の構成のように最終の昇圧段だけを間欠動作させることで出力電圧に影響する昇圧動作によるリップル電圧の発生を抑えることができ、比較部１０８の構成を図５のようにヒステリシスを持たないものを利用しても安定した出力電圧が得られる。

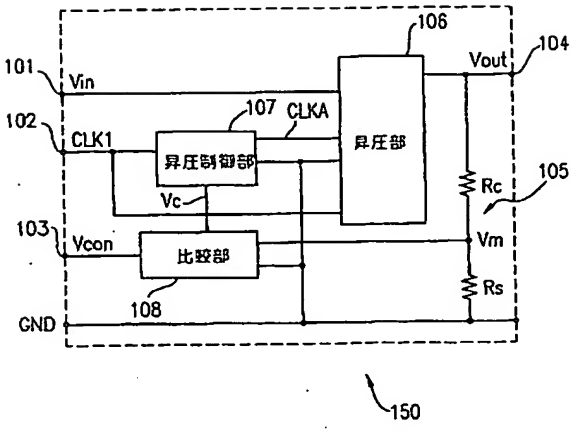
【００６４】消費電力の観点で見ると、前記実施形態１では、全ての昇圧段が間欠動作を行っているのに対し、本実施形態では、第３段の昇圧段のみ間欠動作を行い、その他の昇圧段が常に動作しているため、消費電力の観点から本実施形態が不利であるように思われる。しかしながら、第２段の昇圧段までででは、昇圧された電圧は液晶表示（液晶を駆動する）に必要な電圧以下であり、第２段の昇圧段までが常に動作していることで、第３段の昇圧段の間欠動作の停止時間が長くなる。このため、昇圧回路全体で見ると、本実施形態と、第１の実施形態には消費電力に大きな差はみられない。

【００６５】ここでは、便宜上ＶｃｏｎとＶｍの電位差と周辺の回路動作を添付図面の構成に沿って動作説明を行った。このため、Ｖｃｏｎ＜Ｖｍで昇圧動作が開始され、Ｖｃｏｎ＞Ｖｍのとき昇圧動作が停止する。しかしながら、比較部及び昇圧制御部の論理構成によっては逆の構成にしても問題はない。

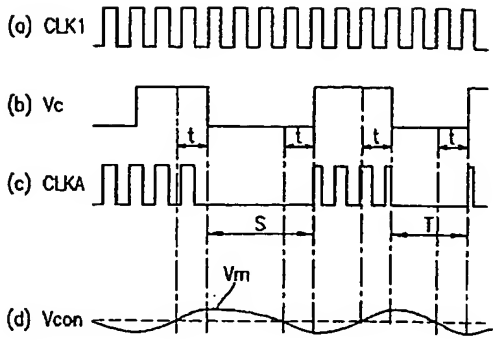
【００６６】

【発明の効果】以上説明したように、本発明の電源回路によれば、比較部が昇圧部の出力電圧と外部から入力される制御電圧とを比較して、その結果を信号出力し、昇圧制御部が動作用クロック信号に従って動作し、比較部からの出力信号に基づく昇圧用クロック信号を昇圧部に供給し、昇圧部が、この昇圧用クロック信号に基づいて、電源からの入力電圧を所定の出力電圧に昇圧する。このため、チャージポンプ方式を用いながら制御電圧により出力電圧を任意に設定することができる。また、比較部からの出力信号に基づいて昇圧制御部が昇圧部の動作を制御し必要以上の昇圧を行わないので、負荷特性に対応する最適な昇圧動作を行うことができる。従って、電源回路全体の電圧変換効率の向上及び消費電力の低減を図ることができる。

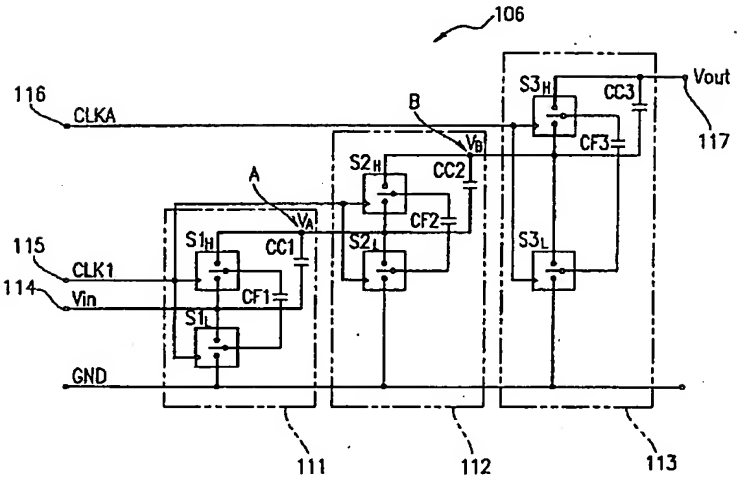
【図１０】


106
Vout
104
101
Vin
107
CLKA
102
CLK1
昇圧制御部
昇圧部
Rc
105
Vc
103
Vcon
比較部
Vm
Rs
108
GND
150

【図１２】


(a) CLK1
(b) Vc
t
(c) CLKA
S
T
Vm
(d) Vcon

【図１１】


106
116
CLKA
B
S3H
CC3
Vout
VB
CF3
117
S2H
CC2
A
VA
CF2
115
CLK1
S1H
CC1
S2L
S3L
114
Vin
CF1
S1L
GND
111
112
113

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.